WHAT IS CLAIMED IS:

1. An integrated circuit for electrostatic discharge (ESD) protection comprising:

a silicon-controlled rectifier (SCR);

a first transistor of a first type integrally formed with the SCR including a first gate;

a second transistor of a second type integrally formed with the SCR including a second gate; and

a control circuit in response to a first voltage applied to the first and second gates providing a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state.

2. The circuit of claim 1, the control circuit further comprising an output terminal coupled to the first and second gates.

3. The circuit of claim 1, the control circuit further comprising a resistor, a capacitor and an output terminal disposed between the resistor and the capacitor.

4. The circuit of claim 1, the control circuit including a resistor-capacitor delay circuit.

5. The circuit of claim 1, the SCR further comprising a p-type substrate, an n-well formed in the p-type substrate, a p-type diffused region formed in the n-well, and an n-type diffused region formed outside of the n-well.

6. The circuit of claim 5, the first transistor further comprising a channel region formed in the n-well.

7. The circuit of claim 5, the second transistor further comprising a channel region formed in the p-type substrate.

8. An integrated circuit for electrostatic discharge (ESD) protection comprising:

a silicon-controlled rectifier (SCR);

a p-type transistor formed integrally with the SCR;

an n-type transistor formed integrally with the SCR;

a control circuit coupled to the p-type and n-type transistors providing a first holding voltage to the SCR to keep the SCR from latching-up, and providing a second holding voltage to the SCR to keep the SCR in the latch-up state.

9. The circuit of claim 8, the control circuit further comprising a resistor, a capacitor and an output terminal disposed between the resistor and the capacitor.

10. The circuit of claim 8, the control circuit further comprising an output terminal coupled to a gate of the p-type transistor and a gate of the n-type transistor.

11. The circuit of claim 8, the SCR further comprising a p-type substrate, an n-well formed in the p-type substrate, a p-type diffused region formed in the n-well, and an n-type diffused region formed outside of the n-well.

12. The circuit of claim 11, the SCR further comprising a different p-type diffused region partially formed in the n-well to serve as a drain of the p-type transistor, wherein the p-type diffused region serves as a source of the p-type transistor.

13. The circuit of claim 11, the SCR further comprising a different n-type diffused region formed in the p-substrate to serve as a drain of the n-type transistor, wherein the n-type diffused region serves as a source of the n-type transistor.

14. The circuit of claim 8, the SCR being coupled between a contact pad and a voltage line.

15. The circuit of claim 8, the SCR being coupled between different voltage lines.

16. An integrated circuit for electrostatic discharge (ESD) protection comprising:

a first voltage line of a first voltage level;

a second voltage line of a second voltage level;

a plurality of contact pads;

a plurality of silicon-controlled rectifiers (SCR), each of the SCRs including a p-type transistor and an n-type transistor integrally formed with the SCR; and

a control circuit providing a first holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs from latching-up, and providing a second holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs in the latch-up state during an ESD event that an ESD pulse appears on the first voltage line or one of the contact pads.

17. The circuit of claim 16, the SCRs further comprising at least one SCR coupled between the first and second voltage lines, and the remaining SCRs each being coupled between a corresponding contact pad and the second voltage line.

18. The circuit of claim 17, wherein during the ESD event, the ESD pulse is discharged from one of the contact pads via the second voltage line to the first voltage line.

19. The circuit of claim 17, wherein during the ESD event, the ESD pulse is discharged from the first voltage line via the second voltage line to one of the contact pads.

20. The circuit of claim 17, wherein during the ESD event, the ESD pulse is discharged from one of the contact pads via the second voltage line to a different contact pad.

21. The circuit of claim 16, the control circuit further comprising a resistor-capacitor delay circuit.

22. The circuit of claim 16, the control circuit further comprising an output terminal coupled to a gate of each of the p-type and n-type transistors.

23. A method of electrostatic discharge protection comprising:

providing a silicon-controlled rectifier (SCR) having a holding voltage;

integrally forming a first transistor of a first type with the SCR including a first gate;

integrally forming a second transistor of a second type with the SCR including a second gate; and

providing a first signal to the first and second gates to raise the holding voltage of the SCR to keep the SCR from latching up; and

providing a second signal to the first and second gates to lower the holding voltage of the SCR to keep the SCR in the latch-up state.

24. The method of claim 23 further comprising raising the holding voltage of the SCR to above a power supply voltage.

25. The method of claim 23 further comprising lowering the holding voltage of the SCR to below a power supply voltage.

26. The method of claim 23 further comprising coupling the SCR between a contact pad a voltage line.

27. The method of claim 23 further comprising coupling the SCR between different voltage lines.

28. A method of providing electrostatic discharge (ESD) protection for internal circuits comprising:

providing a first voltage line of a first voltage level;

providing a second voltage line of a second voltage level;

providing a plurality of contact pads;

providing a plurality of silicon-controlled rectifiers (SCR), each of the SCRs including a p-type transistor and an n-type transistor formed integrally with the SCR; and

providing a first holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs from latching-up, and

providing a second holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs in the latch-up state during an ESD event that an ESD pulse appears on the first voltage line or one of the contact pads.

29. The method of claim 28 further comprising providing the SCRs including at least one SCR coupled between the first and second voltage lines, and the

remaining SCRs each being coupled between a corresponding contact pad and the second voltage line.

30. The method of claim 29 further comprising discharging the ESD pulse from one of the contact pads via the second voltage line to the first voltage line.

31. The method of claim 29 further comprising discharging the ESD pulse from the first voltage line via the second voltage line to one of the contact pads.

32. The method of claim 29 further comprising discharging the ESD pulse from one of the contact pads via the second voltage line to a different contact pad.